In the Claims:

Please amend claims 11, 12 and 16. Please cancel claims 1-10. Please add new claim 27-31. The claims are as follows:

1 -- 10 (Canceled)

11. (Currently Amended) A SDRAM comprising:

at least one bank of DRAM cells;

said SDRAM operable to a first specification defined by a first clock frequency, a first write recovery time and a first time interval for precharge to row address strobe; [[and]]

~~means for programming~~ said SDRAM operable to a second specification defined by a second clock frequency, a second write recovery time and a second time interval for precharge to row address strobe; and

a programmable circuit adapted to control operation of said SDRAM based on said first and said second write recovery times.

12. (Currently Amended) [[The]] A SDRAM ~~of claim 11~~, comprising:

at least one bank of DRAM cells;

said SDRAM operable to a first specification defined by a first clock frequency, a first write recovery time and a first time interval for precharge to row address strobe;

means for programming said SDRAM operable to a second specification defined by a second clock frequency, a second write recovery time and a second time interval for precharge to row address strobe; and

PAGE 5/15 * RCVD AT 5/24/2005 3:16:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):03-28

wherein precharging of bitlines in said at least one bank of DRAM cells is delayed by a time interval substantially equal to the difference between said first write recovery time and said second write recovery time.

13. (Original) The SDRAM of claim 12, wherein said second write recovery time is less than said first write recovery time.

14. (Original) The SDRAM of claim 12, wherein the sum of a minimum internal time to write a DRAM cell of said at least one bank of DRAM cells and a minimum internal time to precharge a bitline connected to said DRAM cell is the same when said SDRAM is operable to said first specification or to said second specification.

15. (Original) The SDRAM of claim 12, wherein the sum of said first write recovery time and said first time interval for precharge to row address strobe is equal to the sum of said second write recovery time and said second time interval for precharge to row address strobe.

16. (Currently Amended) The SDRAM of claim 12, wherein:

said first clock frequency is 1/7.5 nanoseconds, said first write recovery time is 15 nanoseconds and said first time interval for precharge to row address strobe is 15 nanoseconds; and

said second clock frequency is 1/6 nanoseconds, said [[first]] second write recovery time is 15 nanoseconds and said [[first]] second time interval for precharge to row address strobe is 18 nanoseconds.

PAGE 6/15 * RCVD AT 5/24/2005 3:16:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):03-28

17. (Original) A SDRAM comprising:

at least one bank of DRAM cells;

said SDRAM operable to a first write recovery time;

a first circuit for programming said SDRAM operable to a second write recovery time; and

a second circuit for delaying the start of a precharge command for a time interval equal to said first write recovery time when said SDRAM is operable to said second write recovery time.

18. (Original) The SDRAM of claim 17, wherein said SDRAM is operable to a first specification defined by a first clock frequency, said first write recovery time and a first time interval for precharge to row address strobe and said SDRAM is operable to a second specification defined by a second clock frequency, said second write recovery time and a second time interval for precharge to row address strobe.

19. (Original) The SDRAM of claim 18, wherein said first circuit for programming said SDRAM delays precharging of bitlines in said at least one bank of DRAM cells by a time interval substantially equal to the difference between said first write recovery time and said second write recovery time.

20. (Original) The SDRAM of claim 17, wherein said second write recovery time is less than said first write recovery time.

PAGE 7/15 * RCVD AT 5/24/2005 3:16:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):03-28

21. (Original) The SDRAM of claim 17, wherein said first circuit for programming said SDRAM operable to a second write recovery time comprises:

a first delay circuit for receiving and delaying a first timing signal;

a first latch for receiving a first timing signal from said first delay circuit and for latching said first timing signal, said first timing signal indicating a fixed number of data bits have been written to said at least one bank of DRAM cells;

a programmable timer for receiving said first timing signal from said first latch and for delaying said first timing signal by a programmable time interval;

a one shot pulse generator for receiving said first timing signal from said programmable timer and for generating a set signal;

a second latch for receiving said set signal from said one shot pulse generator and for latching said set signal;

a third latch for receiving a second timing signal and for latching said second timing signal, said second timing signal being a signal to turn off wordlines in said at least one bank of DRAM cells;

a logic gate for receiving said set signal from said second latch, for receiving said second timing signal from said third latch and for generating a third timing signal, said third timing signal being a delayed signal to turn off wordlines in said at least one bank of DRAM cells; and

a second delay circuit for receiving and delaying said third timing signal and for simultaneously resetting said first latch, said second latch and said third latch after delaying said third timing signal.

PAGE 8/15 * RCVD AT 5/24/2005 3:16:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):03-28

22. (Original) The SDRAM of claim 21, wherein said programmable timer resets to zero elapsed time upon de-assertion of said first timing signal if said programmable interval has not been reached prior to said de-assertion of said first timing signal

23. (Original) The SDRAM of claim 21, wherein said programmable time interval is determined by a digital signal changing the state of fuses or antifuses.

24. (Original) The SDRAM of claim 21, further including an inverter for receiving said first timing signal, inverting said first timing signal and for applying said inverted timing signal to a reset input of said first latch.

25. (Original) The SDRAM of claim 21, wherein said second delay circuit applies said third timing signal to reset inputs of said first, second and third latches.

26. (Original) The SDRAM of claim 21, wherein said logic gate is an AND gate.

27. (New) The A SDRAM of claim 11, wherein precharging of bitlines in said at least one bank of DRAM cells is delayed by a time interval substantially equal to the difference between said first write recovery time and said second write recovery time.

28. (New) The SDRAM of claim 27, wherein said second write recovery time is less than said first write recovery time.

PAGE 9/15 * RCVD AT 5/24/2005 3:16:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):03-28

29. (New) The SDRAM of claim 27, wherein said SDRAM is operable to the sum of the minimum of said first and second write recovery times and the minimum of said first and second time intervals for precharge to row address strobe.

30. (New) The SDRAM of claim 27, wherein the sum of said first write recovery time and said first time interval for precharge to row address strobe is equal to the sum of said second write recovery time and said second time interval for precharge to row address strobe.

31. (New) The SDRAM of claim 27, wherein:

said first clock frequency is 1/7.5 nanoseconds, said first write recovery time is 15 nanoseconds and said first time interval for precharge to row address strobe is 15 nanoseconds; and

said second clock frequency is 1/6 nanoseconds, said second write recovery time is 15 nanoseconds and said second time interval for precharge to row address strobe is 18 nanoseconds.

PAGE 10/15 * RCVD AT 5/24/2005 3:16:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):03-28